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First Named Inventor	Kim, Hong Koo
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Examiner Name	Marcos D. Pizarro Crespo
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Attorney Docket Number	000939-073311US

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#12 Response

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TOWNSEND and TOWNSEND and CREW LLP

By: _____

AMENDMENT UNDER 37 CFR 1.116
EXPEDITED PROCEDURE –
EXAMINING GROUP 2814

5/6/03

PATENT

Attorney Docket No.: 000939-073311US
Client Ref. No.: P01HA010/US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Hong Koo Kim

Application No.: 09/747,779

Filed: December 22, 2000

For: FABRICATION METHOD AND STRUCTURE FOR FERROELECTRIC NONVOLATILE MEMORY FIELD EFFECT TRANSISTOR

Examiner: Marcos D. Pizarro Crespo

AMENDMENT UNDER 37 CFR 1.116
EXPEDITED PROCEDURE EXAMINING GROUP 2814

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Sir:

In response to the Final Office Action mailed February 25, 2003, please remarks as follows:

REMARKS

Claims 1-24 and 26 are pending. No claim has been amended, canceled, or added.

Claims 1, 3-10, and 14-22 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai and Kirlin. Applicant respectfully traverses the rejection. Claim 1 is directed to a method for fabricating a non-volatile memory device. The claim recites, "providing a substrate; forming an oxide layer overlying the substrate; forming a buffer

layer overlying the oxide layer; thermally annealing the buffer layer to enhance an alignment of crystallites of the buffer layer; forming a ferroelectric material overlying the substrate; forming a gate layer overlying the ferroelectric material, the gate layer overlying a channel region; and forming a first source/drain region adjacent to a first side of the channel region and a second source/drain region adjacent to a second side of the channel region."

The claimed invention recites "thermally annealing the buffer layer to enhance an alignment of crystallites of the buffer layer." In one embodiment, the buffer layer, e.g., MgO, is annealed for about 30 minutes at a temperature of 800-1,000 Celsius to enhance the alignment of the buffer layer in a highly oriented pattern (page 7, lines 9-16). This facilitates growth of a highly oriented ferroelectric layers on the buffer layer.

Hirai does not disclose or suggest the above recited step of "thermally annealing the buffer layer to enhance an alignment of crystallites of the buffer layer." Hirai heats the substrate having a paraelectric oxide film 5 to form a silicon oxide layer 4 underneath the paraelectric oxide film 5 (col. 7, lines 37-43).

Accordingly, the purpose of heating in Hirai is entirely different than the recited features in the claimed invention. Many process steps that have similar names provide widely different results depending on the intended purposes. For example, there are many different ways to deposit a film on a substrate and disclosing one way does not disclose or suggest another deposition method, particularly if the intended purposes of deposition is different, e.g., forming of gate oxide and oxide isolation structures. Similarly, various etch steps are also performed differently according to their intended purposes, e.g., different bias and source powers may be used, different gas mixtures, and different temperatures.

Applicant respectfully note that the heating step disclosed in Hirai appears to be different than the annealing step described in the present application, reflecting the differences in intended purposes of the two steps. That is, Hirai is performed at a temperature from 650 to 750 Celsius for 5-20 minutes (col. 7, lines 37-43), whereas the annealing step is performed at a temperature of 800-1,000 Celsius for about 30 minutes

according to the disclosed embodiment. Perhaps, it is possible that different parameters (e.g., different temperature range and different duration) than one disclosed in the present embodiment could be used for "thermally annealing the buffer layer to enhance an alignment of crystallites of the buffer layer." However, one would have to appreciate the need for such a step to formulate a different set of parameters for performing the annealing step recited in claim 1. Hirai does not disclose or suggest such an appreciation. Kirin et al does not remedy the deficiency of Hirai. Therefore, claim 1 is allowable at least for the reasons set forth above.

Claim 21 recites, "thermally annealing the second buffer layer to enhance an alignment of crystallites of the second buffer layer." Neither Hirai nor Kirin disclose this recited feature. Therefore, claim 21 is allowable.

Claim 2 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hirai, Kirin, and Maiti in view of Yamazaki. Applicant respectfully traverses the rejection. Claim 2 depends from claim 1 and is allowable at least for this reason.

Claims 11 and 12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hirai, Kirin, Maiti further in view of Van Zant and Evetts et al. (US 5361720). Applicant respectfully traverses the rejection. Claims 11 and 12 depend from claim 1 and are allowable at this for this reason.

Claim 13 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hirai, Kirin, Maiti, Van Zant, Evetts and Wolf. Applicant respectfully traverses the rejection. Claim 13 depend from claim 1 and are allowable at this for this reason. In addition, there is no motivation to combine Wolf and Hirai. The temperature and duration of annealing are set according to intended purposes. Hirai discloses a heating step for forming a silicon oxide layer and provides no motivation as to desirability of performing this step at 800-1,000 Celsius. Wolf does not remedy this deficiency.

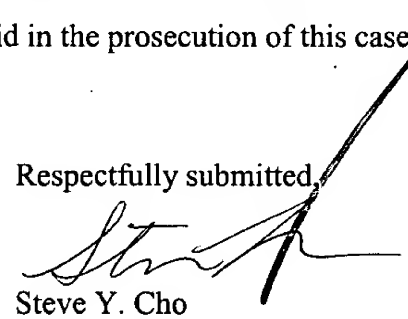
Claims 23 and 24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hirai, Kirin, Maiti in view of Iyer. Applicant respectfully traverses the rejection. These claims depend from claim 21 and are allowable at least for this reason.

Claim 26 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hirai, Kirin, Maiti, and Wolf. Applicant respectfully traverses the rejection. This claim depends from claim 21 and are allowable at least for this reason. In addition, there is no motivation to combine Wolf and Hirai. The temperature and duration of annealing are set according to intended purposes. Hirai discloses a heating step for forming a silicon oxide layer and provides no motivation as to desirability of performing this step at 800-1,000 Celsius. Wolf does not remedy this deficiency.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is urged. If the Examiner believes a telephone conference would aid in the prosecution of this case in any way, please call the undersigned at 650-326-2400.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

All pending claims are provided below for the Examiner's convenience. No claim has been amended or canceled or added.

1. A method for fabricating a non-volatile memory device, the method comprising:

providing a substrate;

forming an oxide layer overlying the substrate;

forming a buffer layer overlying the oxide layer;

thermally annealing the buffer layer to enhance an alignment of crystallites of the buffer layer;

forming a ferroelectric material overlying the substrate;

forming a gate layer overlying the ferroelectric material, the gate layer overlying a channel region; and

forming a first source/drain region adjacent to a first side of the channel region and a second source/drain region adjacent to a second side of the channel region.

2. The method of claim 1 wherein the channel region is about 1 micron and less.

3. The method of claim 1 wherein the ferroelectric material is a PZT bearing compound.

4. The method of claim 1 wherein the buffer layer is a magnesium bearing compound.

5. The method of claim 1 wherein the buffer layer is a magnesium oxide layer, the magnesium oxide layer being a barrier layer.

6. The method of claim 1 wherein the ferroelectric material has a thickness of less than about 1,000 Angstroms.

7. The method of claim 1 wherein the buffer layer has a thickness ranging from about 7 to 100 nanometers.

8. The method of claim 1 wherein the ferroelectric material has a thickness of about 100 Angstroms and greater.

9. The method of claim 1 wherein the ferroelectric material is PZT.

10. The method of claim 1 wherein the buffer layer is a barrier diffusion layer, the barrier diffusion layer substantially preventing diffusion between the ferroelectric material to the substrate.

11. The method of claim 1 wherein the buffer material is sputtered from a substantially pure magnesium target to form a magnesium oxide layer.

12. The method of claim 11 wherein the sputtering is maintained at a temperature greater than about 400 degrees Celsius or greater than about 500 degrees Celsius.

13. The method of claim 11 wherein the buffer layer is thermally annealed at a temperature of 800-1000 degrees Celsius for about 30 minutes.

14. The method of claim 1 wherein the ferroelectric material is highly oriented.

15. The method of claim 14 wherein the highly oriented material is a polycrystalline film.

16. The method of claim 1 wherein the ferroelectric material is substantially free from an amorphous structure.

17. The method of claim 15 wherein the polycrystalline film has a crystal structure of 100 angstroms and greater.

18. The method of claim 1 wherein the buffer layer is a template to provide an oriented growth of the ferroelectric material.

19. The method of claim 1 wherein the oxide layer is provided by a dry oxidation process comprising an oxygen bearing compound.

20. The method of claim 1 wherein the oxide layer passivates the surface of the substrate to protect the channel region.

21. A method for fabricating a non-volatile memory device, the method comprising:

providing a substrate;

forming a first buffer layer overlying the substrate;

forming a second buffer layer overlying the first buffer layer;

thermally annealing the second buffer layer to enhance an alignment of crystallites of the second buffer layer;

forming a ferroelectric material overlying the substrate;

forming a gate layer overlying the ferroelectric material, the gate layer overlying a channel region; and

forming first and second doped regions adjacent to first and second ends of the channel region.

22. The method of claim 21, wherein the first buffer layer is a gate oxide layer, and the second buffer layer is a MgO layer.

23. The method of claim 21, wherein the first buffer layer is an amorphous layer, and the second buffer layer is a highly-oriented layer.

24. The method of claim 23, wherein the second buffer layer has a thickness of no more than 10 nm.

26. The method of claim 21 wherein the second buffer layer is thermally annealed at a temperature of 800-1000 degrees Celsius.